

Articulation and Sharing of Distributed Design Project and Process Knowledge

a short paper



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Tangier, Morocco, September 16, 2010

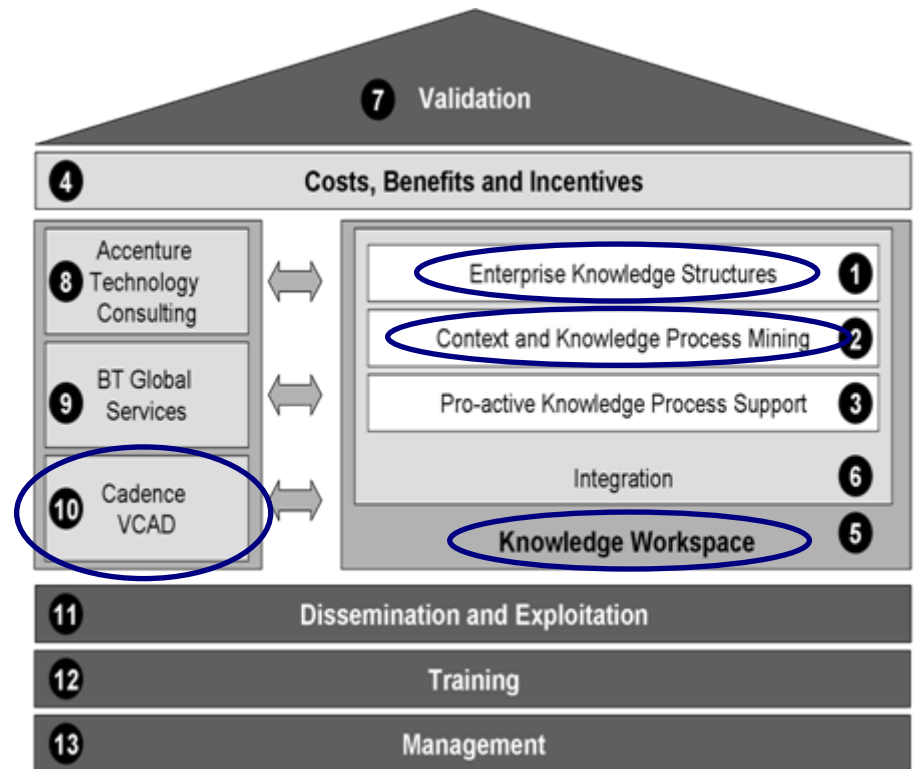
IDC 2010

Agenda

- ▶ Accent pretty much on what is not in the paper
- ...
- ▶ Research in the context of ACTIVE IP
 - Case Study – focus on performance management (informal processes)
- ▶ Approach and Prototype Architecture
- ▶ Implementation Results
- ▶ Knowledge Representation
- ▶ Summary

ACTIVE Integrated Project (FP7)

- ▶ Aim:
 - Increasing the productivity of knowledge workers in a pro-active, contextualized, yet easy and unobtrusive way
- ▶ Approach:
 - Convert tacit and unshared knowledge – the "hidden intelligence" of enterprises – into transferable, interoperable and actionable knowledge to support seamless collaboration and to enable problem solving
- ▶ Focus:
 - Productivity in informal processes



ACTIVE: Informal Processes

- ▶ Informal processes are carried out by knowledge workers with their skills, experience and knowledge, often to perform difficult tasks which require complex, informal decisions among multiple possible strategies to fulfill specific goals
- ▶ In contrast to business processes which are formal, standardized, and repeatable, knowledge processes are often not even written down, let alone denoted formally, vary from person to person to achieve the same objective, and are often not repeatable
- ▶ Knowledge workers create informal processes on the fly in many situations of their daily work

Cadence Design Systems

- ▶ A leader on the Electronic Design Automation (EDA) Market
- ▶ Customers:
 - Systems companies
 - Semiconductor companies
 - Design/supply chain partners
- ▶ Focus:
 - In Development – electronic systems and Integrated Circuits (IC's)
 - In Services: improving the productivity of our customers' design environments
- ▶ Cadence Global Services

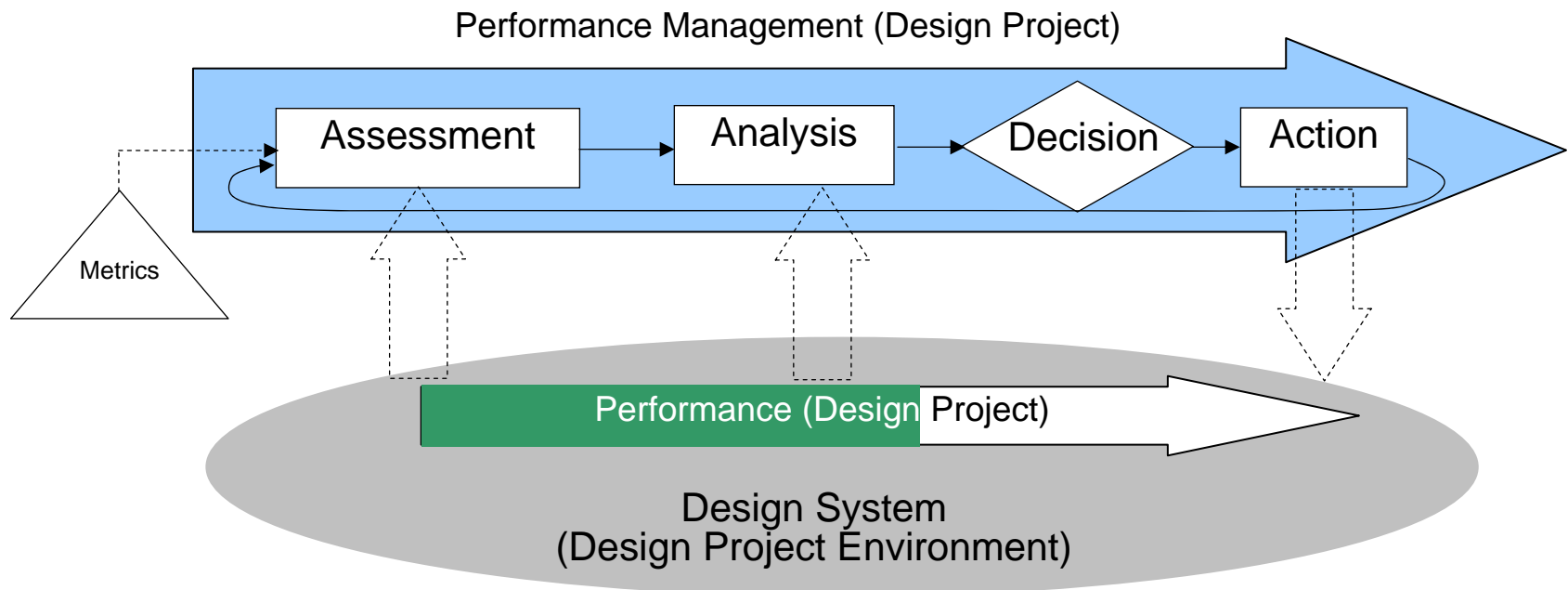


Informal Processes in MIC Design



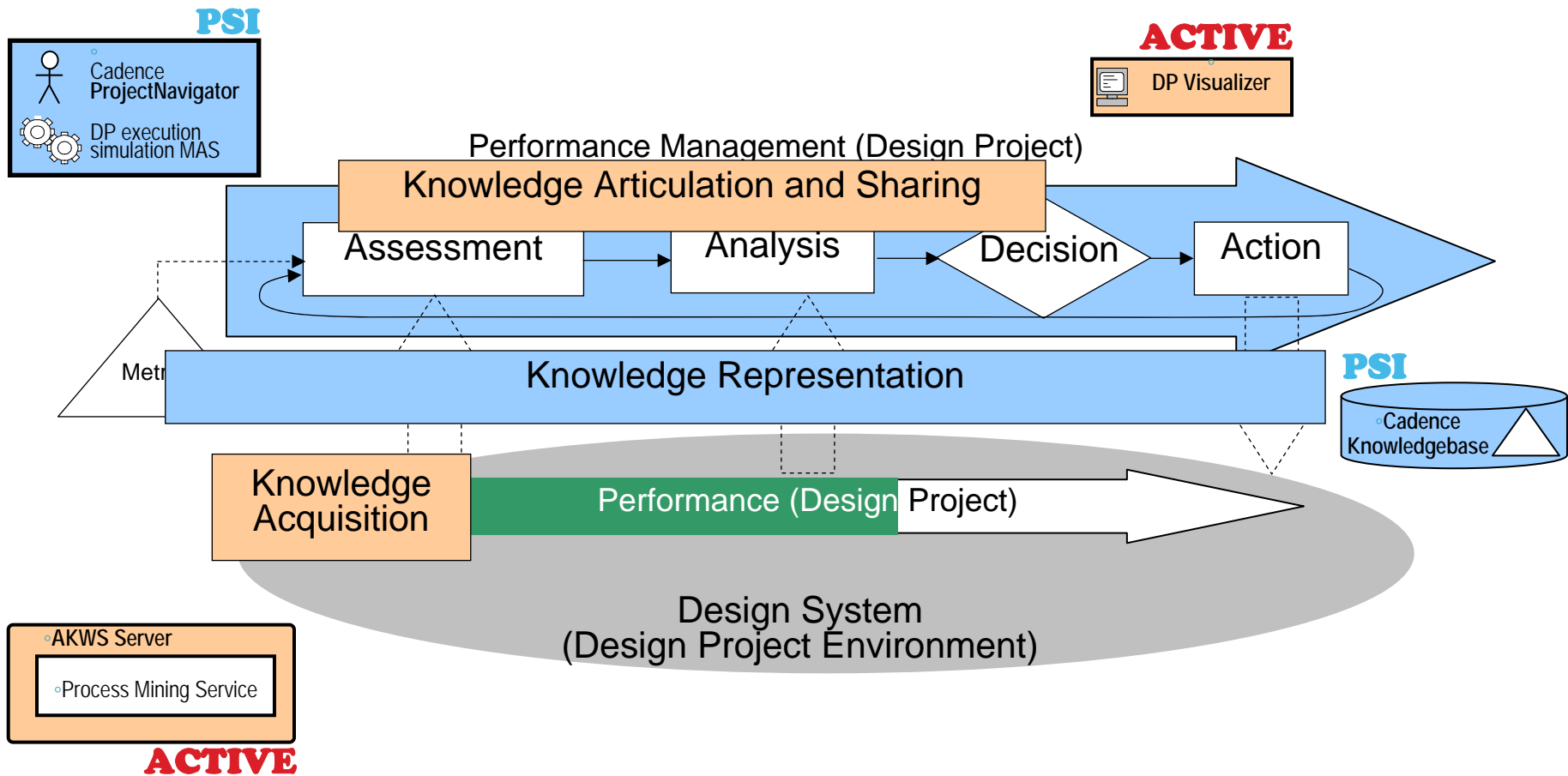
Performance Management

– an Informal Process

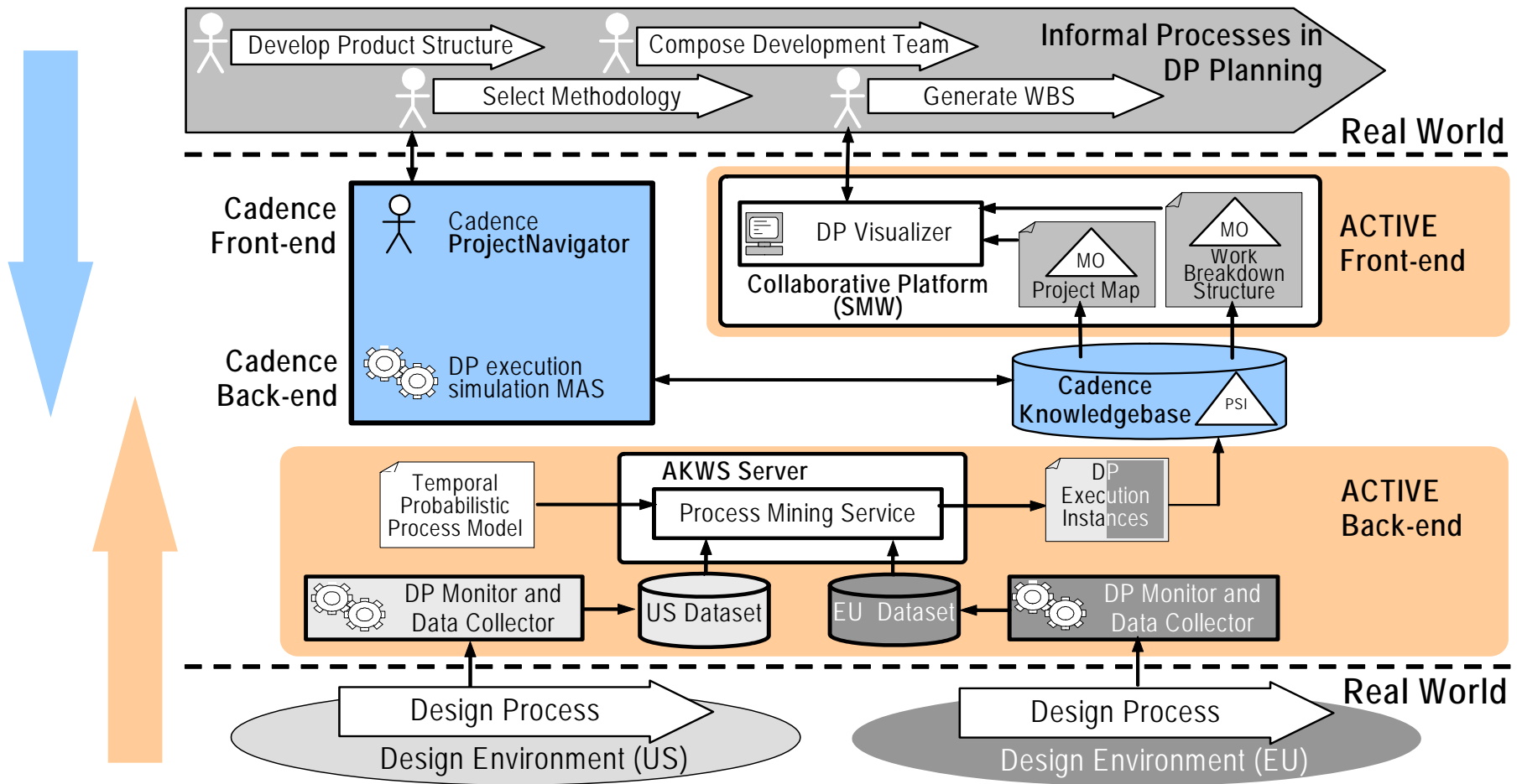


Performance Management

– an Informal Process



Prototype Architecture



↓ Develop Product Structure

Knowledge Articulation and Sharing in DP Visualizer

▶ Visualization

- Links to:
 - Processes
 - Tools
 - Actors

▶ Discussion

- Pro-con summaries
- Discussion threads

▶ LiveNetLife

- Page sharing and chats

The screenshot displays the DP Visualizer web application interface. The top part shows a hierarchical diagram of product structure with nodes for 'pll Analog' and its children: 'pll lf Analog', 'pll iqdiv2 Analog', and 'pll cp Analog'. A blue arrow points from the 'pll lf Analog' node to a discussion thread. The discussion thread is titled 'Talk:Http://psi.vcad-vlab.net/inst/project/tc1?DesignArtifact AEE90812A22CA3DD8' and contains a table of comments.

Comment	User	Role	Status	ProCon	Text
DA Comment5	Vadim Ermolayev	KE	Minor	Pro	So far So Good
DA Comment8	Eyck Jentzsch	Project Manager	Major	Pro	Correspondence to Req Spec
DA Comment10	Wolf-Ekkehard Matzke	Lead Designer (Analog)	Major	Contra	Analog part insufficiently detailed

Below the table, there is a section for 'Functional Block Structure' with the text: 'The structure of the analog part needs to be further elaborated'. At the bottom right, there is a chat window for 'Vadim Ermolayev' with a 'LIVENETLIFE' logo.

Select Development Methodology

and Bind it to the Product Structure

Http://psi.vcad-vlab.net/inst/kb/ds cdns?GenericTask 2

Navigation: Main Page, Community portal, Current events, Recent changes, Random page, Help

Search the wiki: [Go] [Search]

Toolbox: What links here, Related changes, Upload file, Special pages, Printable version, Permanent link, Browse properties

Diagram: Analog Floorplanning (Version 1) is a Successor of MasterTask of tc1. It has an InputConfig (Http://psi.vcad-vlab.net/inst/kb/ds cdns?InputConfig 6) and an OutgoingStatePattern (Floorplan of Analog Layout). It requires the role of Analog Frontend Designer and uses the Virtuoso tool.

Category: GenericTask

Generic

Http://psi.vcad-vlab.net/inst/project/tc1?Task 1

Navigation: Start Page, Community portal, Current events, Recent changes, Random page, Help

Search the wiki: [Go] [Search]

Toolbox: What links here, Related changes, Upload file, Special pages, Printable version, Permanent link, Browse properties

Metadata: belongs to GenericTask: tc1, Version: 1, has Actor: Christoph, has DA: PG, Tools: Virtuoso

Diagram: A complex task flow starting with 'Start' and ending with 'End'. It includes tasks like 'Analog Floorplanning of pll', 'Analog Floorplanning of pll cp', 'Analog Floorplanning of pll iqdiv2', and various 'Analog Layout of pll' tasks.

Category: Task

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Product-Bound

Develop Work Breakdown Structure and Monitor Project Execution

	Resource	Duration	% Comp.	Start Date	End Date
- Design of pll	Christoph	104 Hours	100%	1/2/06	1/6/06
Analog Floorplanning of pll	Christoph	2 Hours	100%	1/2/06	1/2/06
Analog Floorplanning of pll_cp	Christoph	3 Hours	100%	1/2/06	1/2/06
Analog Floorplanning of pll_iqdiv2	Christoph	3 Hours	100%	1/2/06	1/2/06
Analog Layout of pll_cp_dni	Christoph	1 Hour	100%	1/2/06	1/2/06
Analog Layout of pll_cp_iqgen	Christoph	1 Hour	100%	1/3/06	1/3/06
Analog Layout of pll_cp	Christoph	1 Hour	100%	1/4/06	1/4/06
Analog Layout of pll_iqdiv2	Christoph	1 Hour	100%	1/4/06	1/4/06
Analog Layout of pll_tf	Christoph	1 Hour	100%	1/4/06	1/4/06
Analog Layout of pll	Christoph	1 Hour	100%	1/6/06	1/6/06

Powered by [jsGantt](#) Format: Hour Day Week Month

Category: Task

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Design of pll

belongs to: [Design](#)

GenericTask: [Design](#)

Version: 1

has Actor: [Christoph](#)

has DA: [pll](#)

Planned Start Date: 01-Jan-2006 00:00:00

Planned Finish Date: 05-Jan-2006 11:00:00

Tools

Virtuoso

[MS Project XML export](#)

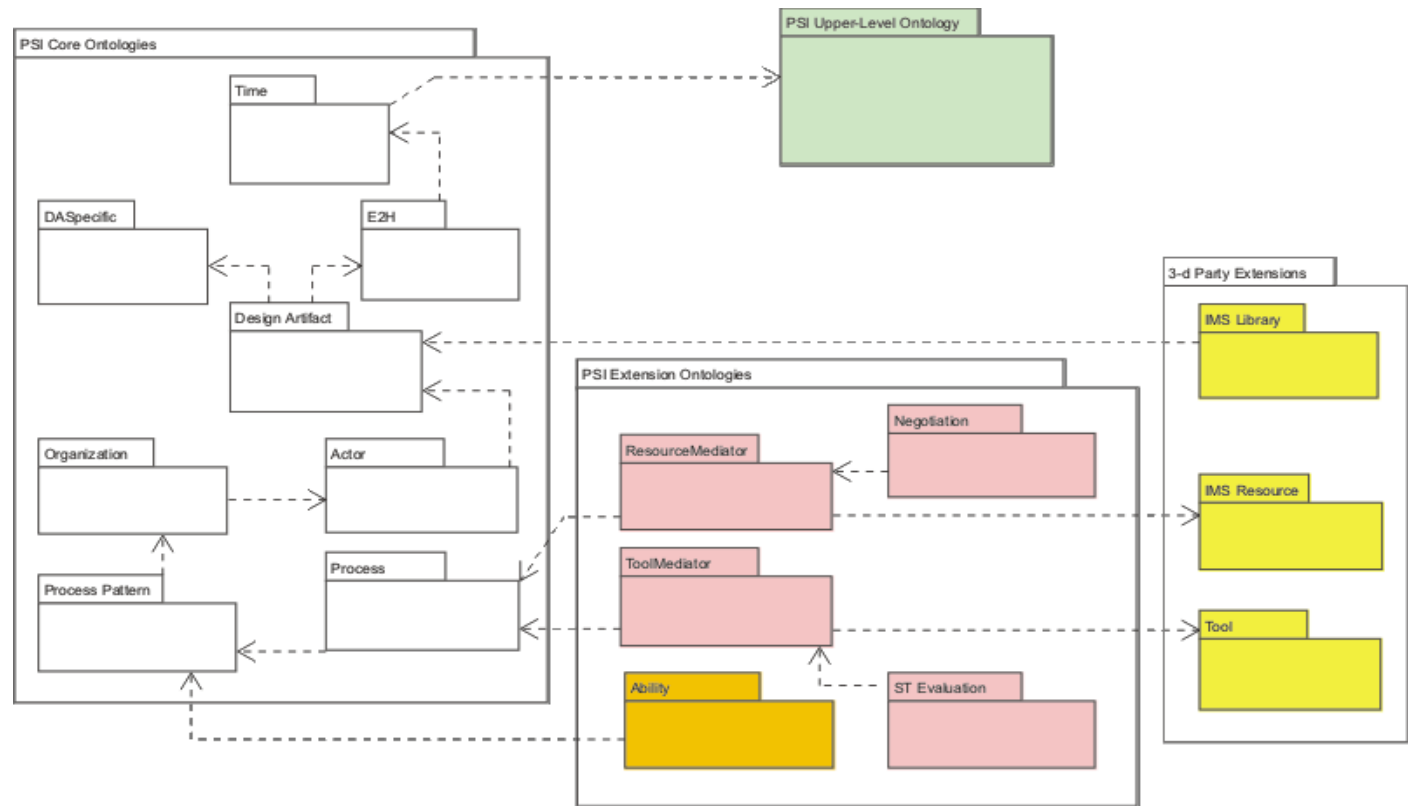
[Back to all Cadence processes](#)

[Vadim Ermolayev: <enter chat here>](#)

[Http://psi.vcad-vlab.net/inst/project/tc1](#) **LIVENETLIFE**

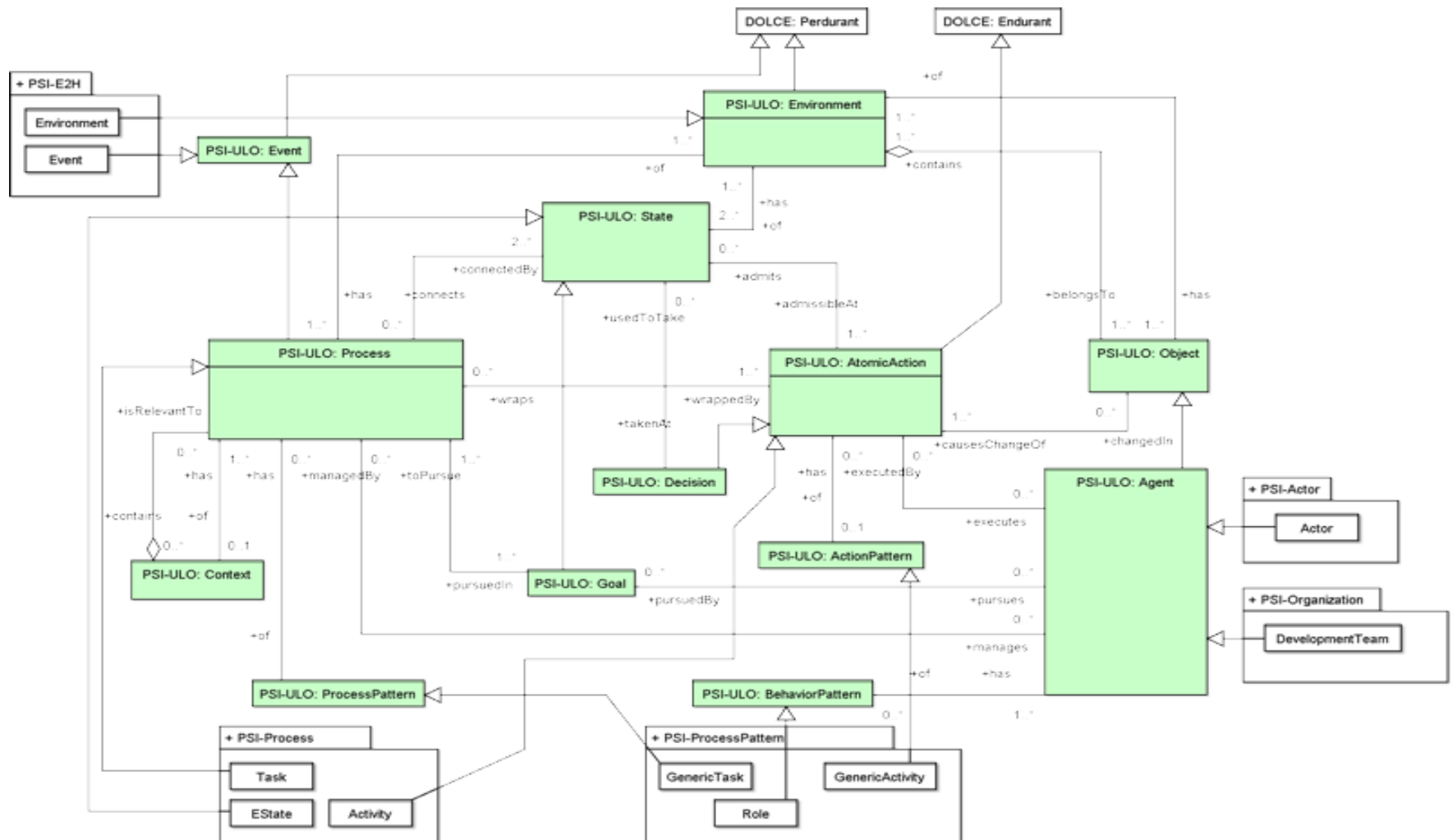
Knowledge Representation

- ▶ PSI Suite of Ontologies v.2.3
- ▶ OWL-DL



- ▶ [http://isrg.kit.znu.edu.ua/ontodocwiki/index.php/PSI Suite of Ontologies](http://isrg.kit.znu.edu.ua/ontodocwiki/index.php/PSI_Suite_of_Ontologies)

KR: PSI-ULO – Process Context



Summary

- ▶ Tacit (and distributed) knowledge acquisition articulation and sharing in MIC Engineering Design Projects
- ▶ Back-End: ACTIVE Knowledge WorkSpace
- ▶ Front-End: ACTIVE Design Project Visualizer
 - Paper – Demonstrator Prototype
 - Currently – Fully Functional Prototype
 - E.g. (front-end) Gantt chart visualization for WBS, execution monitoring, ...
- ▶ Planned future work (short term):
 - Validation with industrial users

Questions Please ...

